REMARKS

This Amendment is filed in response to the Office Action dated July 7, 2005. For the following reasons this application should be allowed and the case passed to issue. No new matter is introduced by this Amendment. The amendments to the claims are supported throughout the specification. For example, the amendment to claim 1 is supported by specification at page 6, lines 10-30, which teaches an n-type well region 2a in Fig. 2A corresponding to "a first well," and an n-type well region 2b in Fig. 2B corresponding to "a second well." New claim 11 is supported by the specification at page 10, lines 19-26. Figs. 7A and 7B, clearly disclose a p-type semiconductor substrate 1, a pair of p-type impurity diffused regions 3, a floating gate 5, and n-type impurity diffused control region 11. The n-type impurity diffused regions 11 are a pair of source/drain impurity diffused regions formed at a main surface of the p-type semiconductor substrate 1 such that a region of the p-type semiconductor substrate 1 positioned below the floating gate 5 is interposed between the paired source/drain impurity diffused regions.

Claims 1-11 are pending in this application. Claims 1and 2 have been rejected. Claims 3-10 have been withdrawn pursuant to an election of species requirement. Claims 1, 5, 7, 9, and 10 have been amended in this response. New claim 11 has been added.

Election of Species

Upon the allowance of a claim, Applicants respectfully request consideration and allowance of withdrawn claims 3-10 in accordance with 37 C. F. R. § 1.141.

In addition, Applicants request consideration and allowance of new claim 11.

Claim Rejections Under 35 U.S.C. § 102

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chang (U.S. Patent No. 5,761,121). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention, as claimed, and the cited prior art.

An aspect of the present invention, per claim 1, is a nonvolatile semiconductor memory device comprising a semiconductor substrate having a main surface. A first well and a second well are both formed at the semiconductor substrate. A pair of p-type impurity diffused regions are formed at the first well to serve as source/drain. A floating gate is formed on a region of the semiconductor substrate lying between the paired p-type impurity diffused regions with a tunnel insulating layer interposed between the floating gate and the semiconductor substrate. An impurity diffused control region is formed at the second well to control a potential of the floating gate.

The Examiner asserted that Chang (Figs. 2 and 3A) discloses a non-volatile semiconductor memory device comprising a semiconductor substrate (14), a pair of p-type impurity diffused regions (20, 22), a floating gate (26), tunnel insulating layer (34), and a p-type impurity diffused control region (36).

Chang, however, does not anticipate the claimed nonvolatile semiconductor memory device. Claim 1 requires both a pair of p-type impurity diffused regions formed at a first well to serve as source/drain, and an impurity diffused control region formed at a second well to control a potential of the floating gate.

In contrast thereto, Chang does not disclose a nonvolatile semiconductor memory device including both a pair of p-type impurity diffused regions formed at a first well to serve as source/drain, and an impurity diffused control region formed at a second well to control a potential of the floating gate, as required by claim 1. Referring to Figs. 2 and 3A of Chang the diffusion regions 20, 22 and the control gate 36 are not formed in different wells; both are formed in N-well 12. Therefore, Chang does not disclose a nonvolatile semiconductor memory device including both a pair of p-type impurity diffused regions formed at a first well to serve as source/drain, and an impurity diffused control region formed at a second well to control a potential of the floating gate, as required by claim 1.

According to the nonvolatile semiconductor memory device of the present invention, a withstand pressure between the impurity diffused control region and the first well, and the width of a depletion layer formed between the impurity diffused control region and the first well are controllable based on the impurity concentration of the first well. Furthermore, the performance of a floating gate transistor formed of the pair of p-type impurity regions serving as source/drain is controllable based on the impurity concentration of the second well. Therefore, by separately adjusting the impurity concentrations of the first well and the second well, the withstand pressure between the impurity diffused control region and the first well and the width of the depletion layer between the impurity diffused control region and the first well, and the performance of the floating gate transistor can be set in separate, independent, and arbitrary manners.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994); *Hoover Group, Inc. v.*

Custom Metalcraft, Inc., 66 F.3d 399, 36 USPQ2d 1101 (Fed. Cir. 1995); *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). Because Chang does not disclose a pair of p-type impurity diffused regions formed at a first well to serve as source/drain, and an impurity diffused control region formed at a second well to control a potential of the floating gate, as required by claim 1, Chang does not anticipate claim 1.

Applicants further submit that Chang does not suggest the claimed nonvolatile semiconductor memory device.

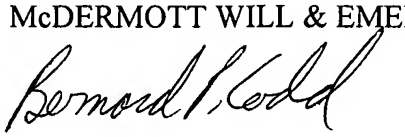
The dependent claims are allowable for at least the same reasons as the independent claims from which they depend and further distinguish the claimed invention. For example, claim 2 further requires that the impurity diffused control region is of p-conductivity type and faces the floating gate with an insulating layer interposed therebetween. Chang does not suggest the claimed nonvolatile semiconductor memory device with this additional limitation.

In light of the above Amendment and Remarks, this application should be allowed and the case passed to issue. If there are any questions regarding these remarks or the application in general, a telephone call to the undersigned would be appreciated to expedite prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Bernard P. Codd
Registration No. 46,429

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BPC:kap
Facsimile: 202.756.8087
Date: October 7, 2005

Please recognize our Customer No. 20277 as our correspondence address.